REMARKS

By the present amendment and response, claims 1 and 14 have been amended to overcome the Examiner's objections. Claims 1, 3-15, 17-23, and 25 are pending in the present application. Reconsideration and allowance of pending claims 1, 3-15, 17-23, and 25 in view of the following remarks are requested.

The Examiner has rejected claims 1, 3-15, 17-23, and 25 under 35 USC §103(a) as being unpatentable over U.S. patent number 5,436,177 to Chiara Zaccherini ("Zaccherini") in view of Shao. For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claims 1 and 14, is patentably distinguishable over Zaccherini and Shao, singly or in combination.

The present invention, as defined by amended independent claim 1, teaches, among other things, doping a layer over a transistor gate region with a first dopant, doping the layer over the transistor gate region and a field oxide region with a second dopant, and doping a portion of the layer over the field oxide region with a third dopant so as to form a high-doped region in the layer over the field oxide region, where the first dopant has a first conductivity type and the second and third dopants have a second conductivity type, and where the transistor gate region is situated over a well and the field oxide region is not situated over the well. As disclosed in the present application, a first dopant, e.g. an N type dopant, is utilized to implant a gate region of a polycrystalline layer, while a doping barrier prevents the first dopant from being implanted in a resistor region of the polycrystalline layer. As disclosed in the present application, the doping

barrier is removed and a second dopant, e.g. a P type dopant, is implanted in the polycrystalline layer to determine the resistivity of a resistor subsequently formed in the resistor region of the polycrystalline layer.

As disclosed in the present application, after formation of a high resistivity resistor in the resistor region of the polycrystalline layer, a silicide blocking layer is formed over the resistor region while leaving a portion of the resistor region uncovered by the silicide blocking layer. P+ doped regions are then formed by heavily doping the uncovered portions of the resistor region of the polycrystalline layer with a third dopant, e.g. a P type dopant having the same conductivity type as the second dopant, and silicide contact regions are formed over the P+ regions so as to provide electrical connectivity for the high resistivity resistor. As a result, the present invention advantageously achieves a high resistivity resistor having a low fabrication cost and improved electrical connectivity.

In contrast to the present invention as defined by amended independent claim 1, Zaccherini does not teach, disclose, or suggest doping a layer over a transistor gate region with a first dopant, doping the layer over the transistor gate region and a field oxide region with a second dopant, and doping a portion of the layer over the field oxide region with a third dopant so as to form a high-doped region in the layer over the field oxide region, where the first dopant has a first conductivity type and the second and third dopants have a second conductivity type, and where the transistor gate region is situated over a well and the field oxide region is not situated over the well. Zaccherini specifically discloses forming P doped resistors in predetermined area 8 of polycrystalline

layer 7 overlying field oxide 5, which is situated on doped epitaxial layer 3. See, for example, column 3, lines 15-23 and Figure 4 of Zaccherini. In Zaccherini, transistor 1 is formed on doped epitaxial layer 3, which covers substrate 2. See, for example, column 2, lines 54-55 and Figure 4 of Zaccherini. Thus, in Zaccherini, predetermined area 8 and transistor 1 are both situated on epitaxial layer 3. However, Zaccherini fails to teach, disclose, or suggest a transistor gate region situated over a well and a field oxide region, over which a high resistivity resistor is formed, not being situated over the well.

Additionally, Zaccherini fails to teach, disclose, or suggest doping a portion of a layer over a field oxide region with a dopant so as to form a high-doped region in the layer over the field oxide region and fabricating a contact region for a high resistivity resistor over the high-doped region. Moreover, Zaccherini provides no motivation for forming a high-doped region in the layer over the field oxide region or even mention any method of completing formation of resistors in predetermined area 8 of polycrystalline layer 7.

In contrast to the present invention as defined by amended independent claim 1, Shao does not teach, disclose, or suggest doping a layer over a transistor gate region with a first dopant, doping the layer over the transistor gate region and a field oxide region with a second dopant, and doping a portion of the layer over the field oxide region with a third dopant so as to form a high-doped region in the layer over the field oxide region, where the first dopant has a first conductivity type and the second and third dopants have a second conductivity type, and where the transistor gate region is situated over a well and

the field oxide region is not situated over the well. Shao specifically discloses performing N+ implant 18 into poly 2 layer 16 to form the conductivity level of an NMOS poly gate and also to control the value of a load resistor, i.e. load resistor 38, which is also formed in poly 2 layer 16 over field oxide region 12. See, for example, column 5, lines 7-26 and Figures 1 and 5 of Shao. In Shao, NMOS gate 40 and load resistor 38 are both situated over substrate 10. See, for example, Figure 5 of Shao. However, Shao fails to teach, disclose, or suggest a transistor gate region situated over a well and a field oxide region, over which a high resistivity resistor is formed, not being situated over the well.

Also, Shao does not teach, disclose, or suggest doping poly 2 layer 16 with a second dopant so as to form a high resistivity resistor in poly 2 layer 16 over field oxide region 12, as specified in amended independent claim 1. Moreover, in Shao, a doping barrier is not utilized above the layer over field oxide region 12, i.e. the resistor region, as specified in amended independent claim 1.

In Shao, after load resistor 38 has been formed, an N+ implant of contact regions 72 and 74 of load resistor 38 is performed. See, for example, column 7, lines 64-65 and Figure 6 of Shao. However, Shao fails to teach, disclose, or suggest utilizing a first dopant to dope a transistor gate region, utilizing a second dopant to form a high resistivity resistor in a layer over a field oxide region, and utilizing a third dopant to form a high-doped region in the layer over the field oxide region, where the first dopant has a first conductivity type and the second and third dopants have a second conductivity type.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by amended independent claim 1, is not suggested, disclosed, or taught by Zaccherini and Shao, singly or in combination. As such, the present invention, as defined by amended independent claim 1, is patentably distinguishable over Zaccherini and Shao. Thus claims 3-13 depending from amended independent claim 1 are, *a fortiori*, also patentably distinguishable over Zaccherini and Shao for at least the reasons presented above and also for additional limitations contained in each dependent claim.

The present invention, as defined by amended independent claim 14, teaches, among other things, doping a polycrystalline silicon layer over a gate region with a first dopant, doping the polycrystalline silicon layer over the gate region and a resistor region with a second dopant, and doping a portion of the resistor region of the polycrystalline silicon layer with a third dopant so as to form a high-doped region in the resistor region, where the first dopant has a first conductivity type and the second and third dopants have a second conductivity type, and where the gate region is situated over a well and the resistor region is not situated over the well. Amended independent claim 14 includes similar limitations as recited in amended independent claim 1. Thus, for similar reasons as discussed above, Applicant respectfully submits that the present invention, as defined by amended independent claim 14, is not suggested, disclosed, or taught by Zaccherini and Shao. As such, the present invention, as defined by amended independent claim 14, is patentably distinguishable over Zaccherini and Shao. Thus claims 15, 17-23, and 25 depending from amended independent claim 14 are, *a fortiori*, also patentably

distinguishable over Zaccherini and Shao for at least the reasons presented above and also for additional limitations contained in each dependent claim.

Based on the foregoing reasons, the present invention, as defined by amended independent claims 1 and 14 and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 1, 3-15, 17-23, and 25 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 1, 3-15, 17-23, and 25 pending in the present application is respectfully requested.

Respectfully Submitted,
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